Arbadell CPU Control State Machine
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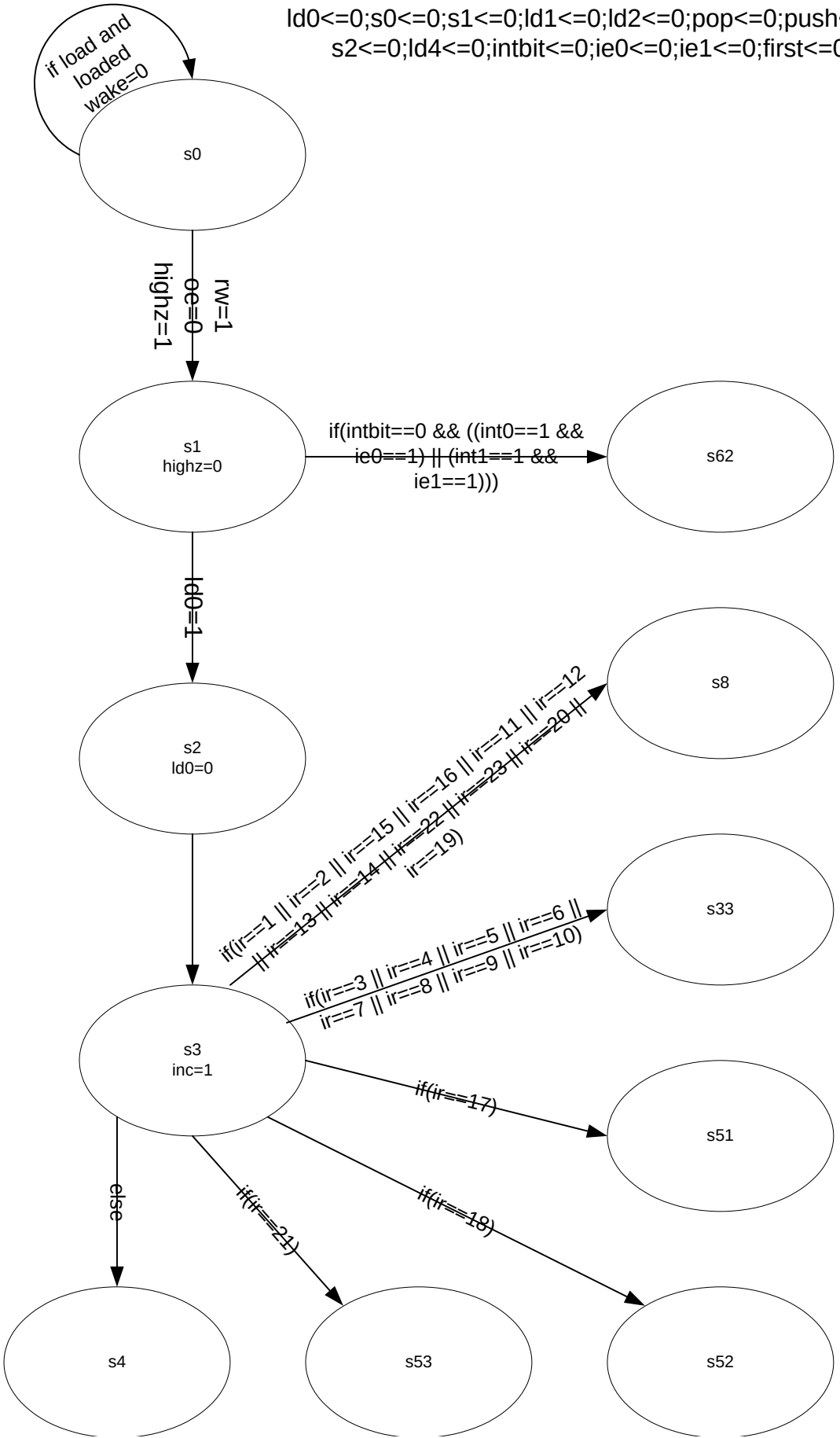
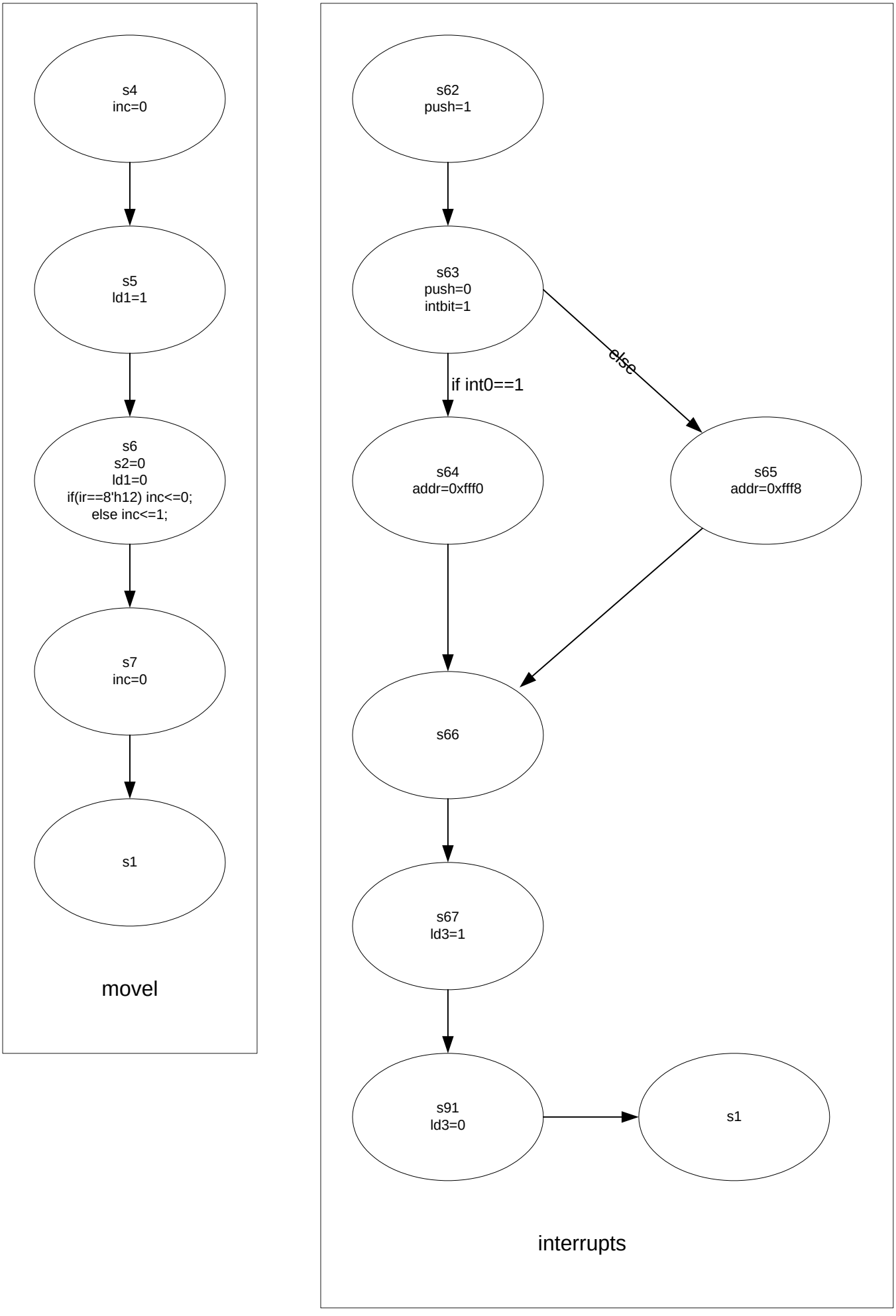
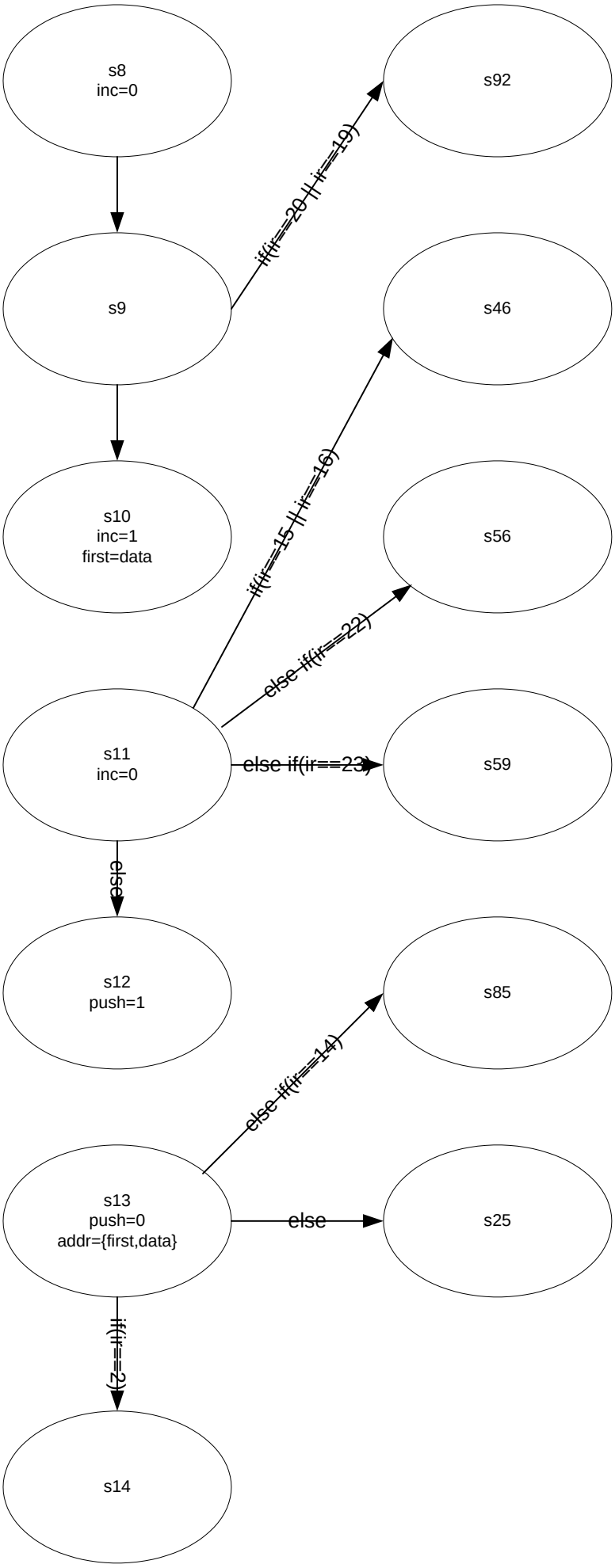
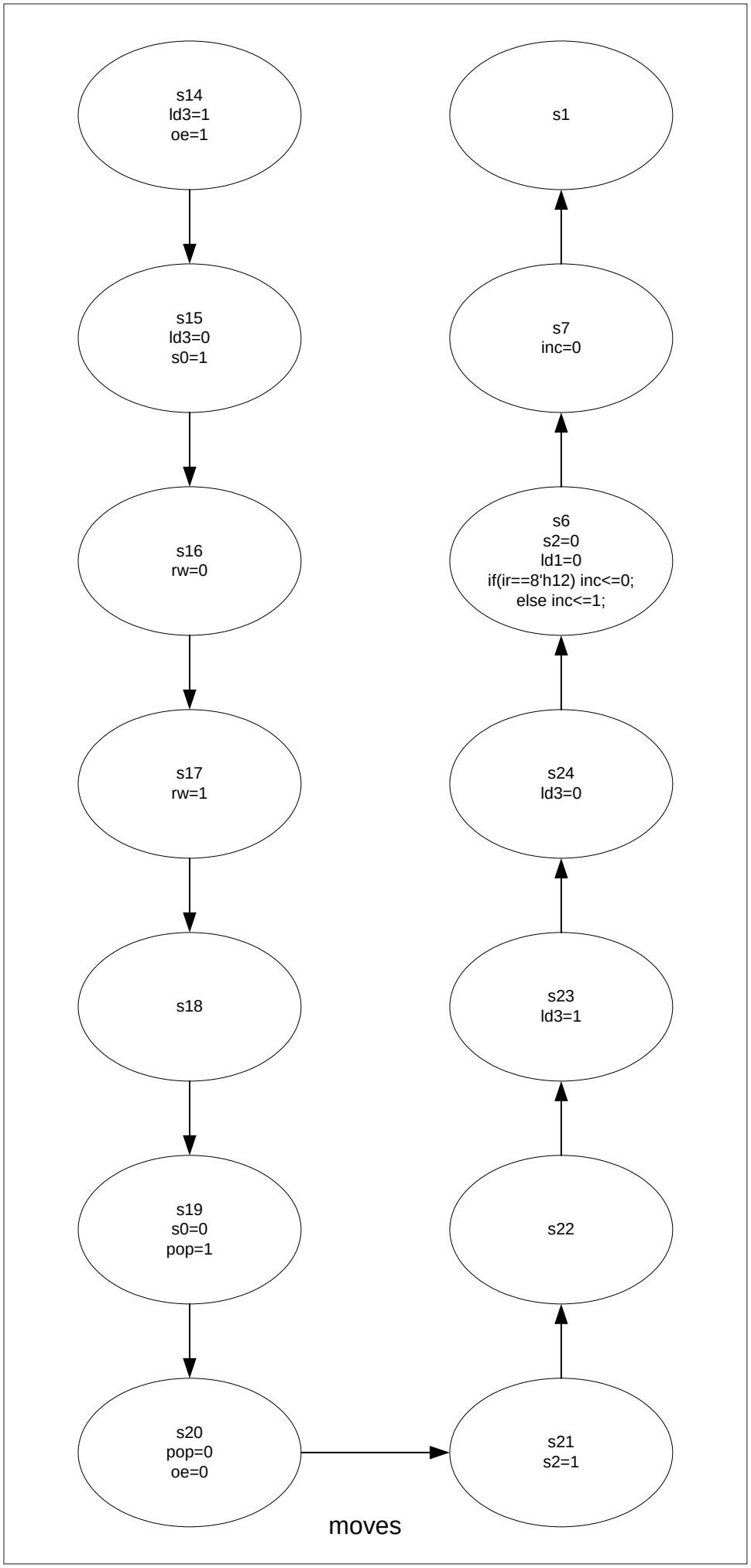
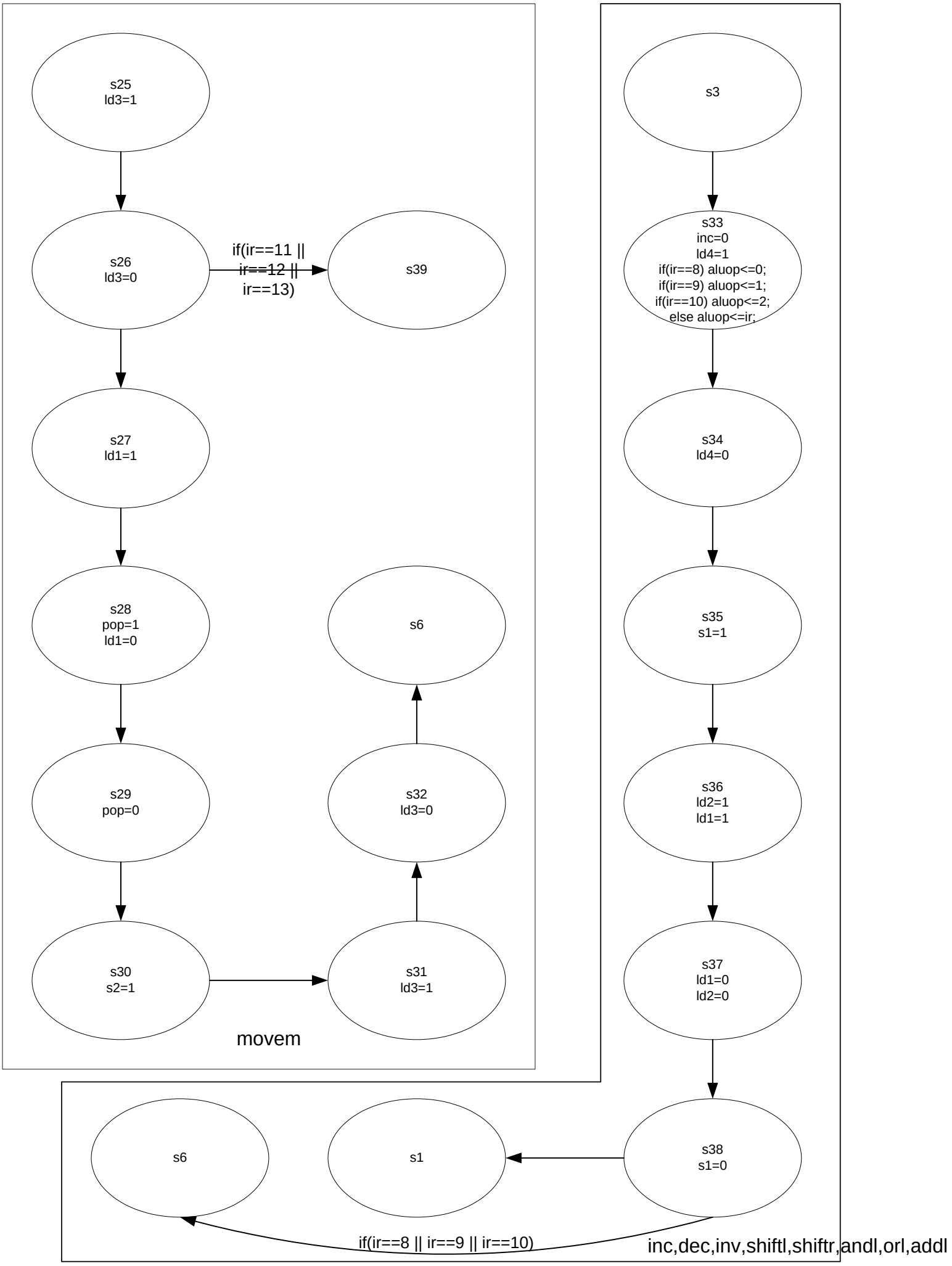
at reset do the following:
state<=0;rw<=1'bz;oe<=1'bz;wake<=1;ioaddr<=0;inc<=0;ld3<=0;
ld0<=0;s0<=0;s1<=0;ld1<=0;ld2<=0;pop<=0;push<=0;highz<=0;
s2<=0;ld4<=0;intbit<=0;ie0<=0;ie1<=0;first<=0;addr<=0;

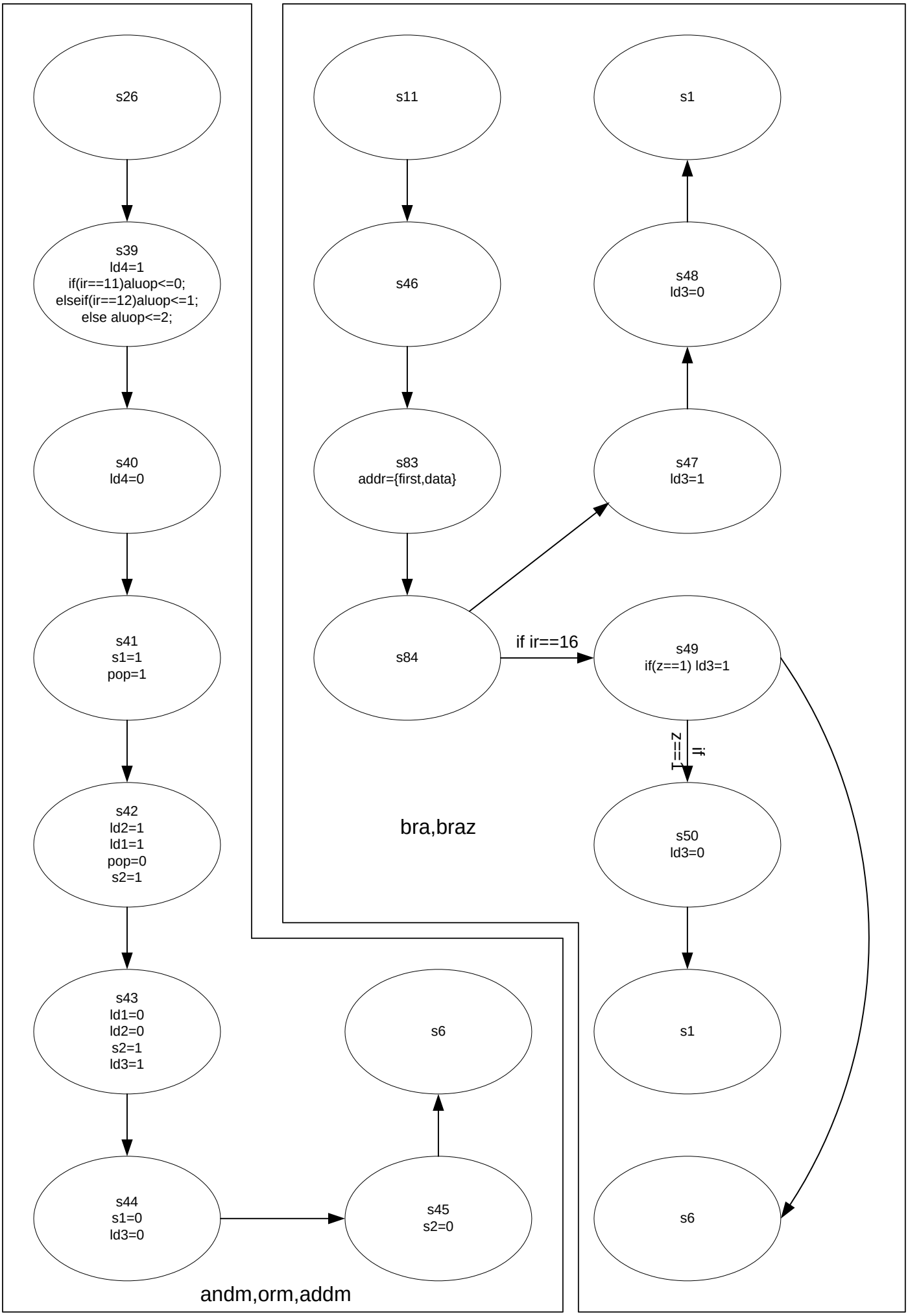


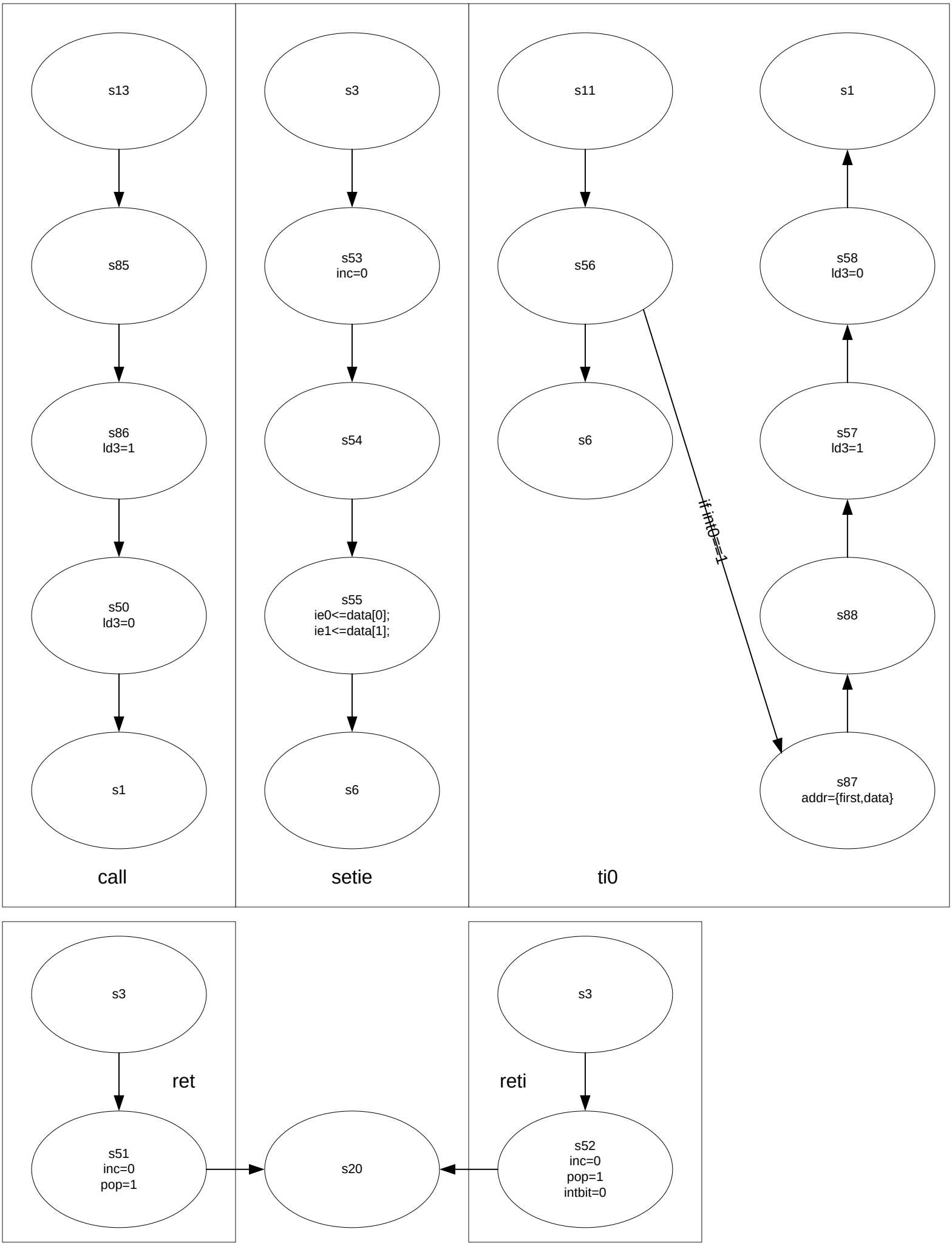

s4
inc=0
s5
ld1=1
s6
s2=0
ld1=0
if(ir==8'h12) inc<=0;
else inc<=1;
s7
inc=0
s1
movel
s62
push=1
s63
push=0
intbit=1
if int0==1
else
s64
addr=0xfff0
s65
addr=0xfff8
s66
s67
ld3=1
s91
ld3=0
s1
interrupts

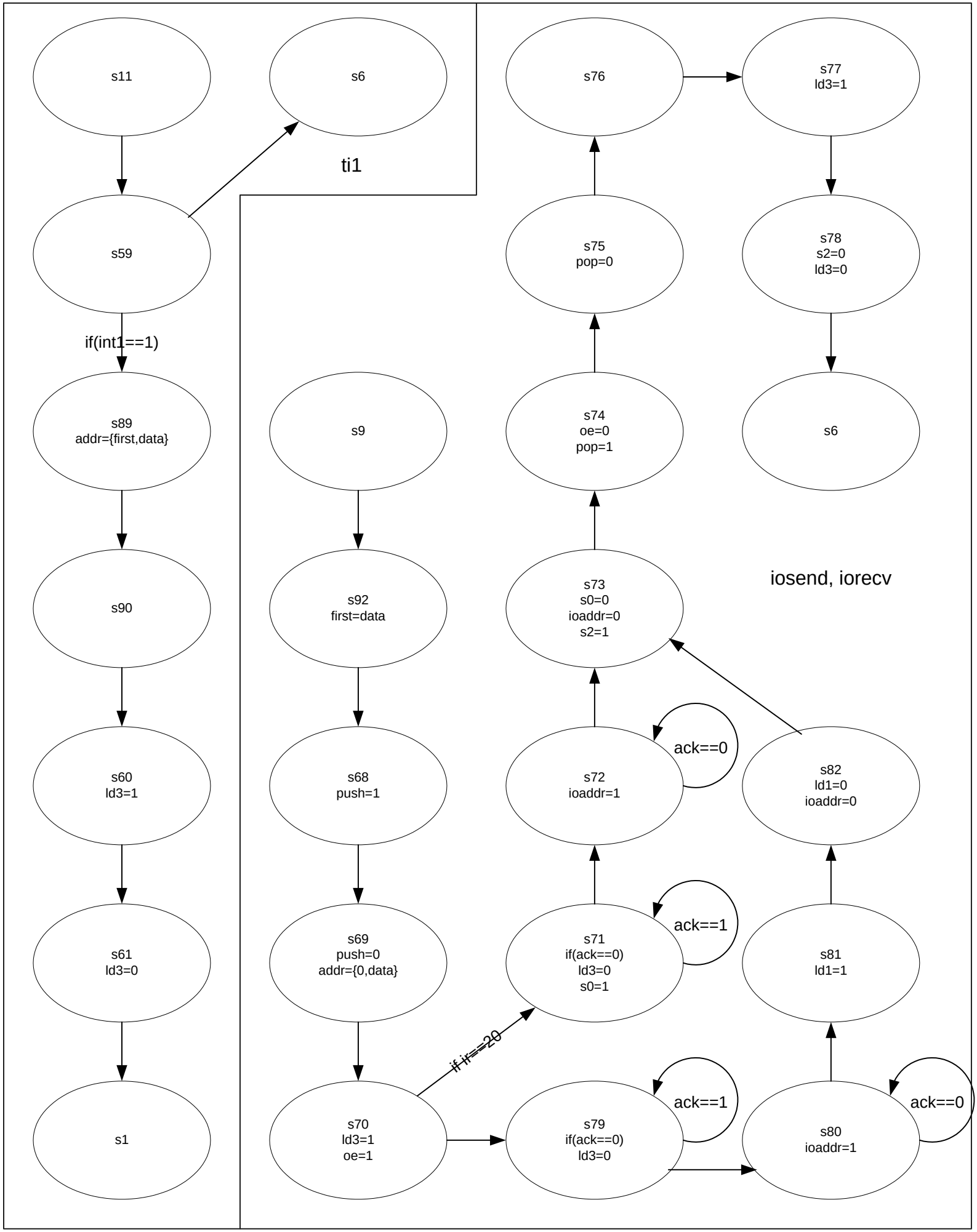

s8
inc=0
s92
if(ir==20 || ir==19)
s9
s46
s10
inc=1
first=data
if(ir==15 || ir==16)
s56
else if(ir==22)
s11
inc=0
else if(ir==23)
s59
else
s12
push=1
s85
else if(ir==14)
s13
push=0
addr={first,data}
else
s25
if(ir==2)
s14


s14
ld3=1
oe=1
s15
ld3=0
s0=1
s16
rw=0
s17
rw=1
s18
s19
s0=0
pop=1
s20
pop=0
oe=0
s21
s2=1
s22
s23
ld3=1
s24
ld3=0
s6
s2=0
ld1=0
if(ir==8'h12) inc<=0;
else inc<=1;
s7
inc=0
s1
moves


s25
ld3=1
s26
ld3=0
if(ir==11 ||
ir==12 ||
ir==13)
s39
s27
ld1=1
s28
pop=1
ld1=0
s6
s29
pop=0
s32
ld3=0
s30
s2=1
s31
ld3=1
movem
s3
s33
inc=0
ld4=1
if(ir==8) aluop<=0;
if(ir==9) aluop<=1;
if(ir==10) aluop<=2;
else aluop<=ir;
s34
ld4=0
s35
s1=1
s36
ld2=1
ld1=1
s37
ld1=0
ld2=0
s38
s1=0
s6
s1
if(ir==8 || ir==9 || ir==10)
inc,dec,inv,shiftl,shiftr,andl,orl,addl


s26
s39
ld4=1
if(ir==11)aluop<=0;
elseif(ir==12)aluop<=1;
else aluop<=2;
s40
ld4=0
s41
s1=1
pop=1
s42
ld2=1
ld1=1
pop=0
s2=1
s43
ld1=0
ld2=0
s2=1
ld3=1
s44
s1=0
ld3=0
s6
s45
s2=0
andm,orm,addm
s11
s46
s83
addr={first,data}
s84
if ir==16
s49
if(z==1) ld3=1
if
T==Z
s50
ld3=0
s1
s6
bra,braz
s1
s48
ld3=0
s47
ld3=1


s13
s85
s86
ld3=1
s50
ld3=0
s1
call
s3
s53
inc=0
s54
s55
ie0<=data[0];
ie1<=data[1];
s6
setie
s11
s56
s6
if int0=1
s1
s58
ld3=0
s57
ld3=1
s88
s87
addr={first,data}
ti0
s3
ret
s51
inc=0
pop=1
s20
s3
reti
s52
inc=0
pop=1
intbit=0


s11
s6
ti1
s59
if(int1==1)
s89
addr={first,data}
s90
s60
ld3=1
s61
ld3=0
s1
s9
s92
first=data
s68
push=1
s69
push=0
addr={0,data}
s70
ld3=1
oe=1
if ir==20
s76
s77
ld3=1
s75
pop=0
s78
s2=0
ld3=0
s74
oe=0
pop=1
s6
s73
s0=0
ioaddr=0
s2=1
iosend, iorecv
s72
ioaddr=1
ack==0
s82
ld1=0
ioaddr=0
s71
if(ack==0)
ld3=0
s0=1
ack==1
s81
ld1=1
s79
if(ack==0)
ld3=0
ack==1
s80
ioaddr=1
ack==0