Arbadell Video Technical Document

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The video portion of Arbadell is handled by two chips. The first is a Xilinx CPLD which will read from external SRAM and display the contents through the VGA interface. It simply rolls through the SRAM starting at byte 0 and reads the SRAM. The SRAM control signals are handled by the PIC. The CPLD will shift out the byte one bit at a time to the VGA RGB signals along with the HSYNC and VSYNC signals. If the PIC needs to write to memory then the CPLD will receive a CLEARING signal which will force the CPLD to give up the address bus.

The second chip involved is the PIC. It will act as an interface between the chipset and the CPLD/SRAM. The PIC will be given a signal from the chipset indicating that there is an ASCII character to be written to SRAM. The PIC will then store the ASCII value into internal RAM and tell the chipset to continue. It will then reference a lookup table to determine what pixels should be written to create the character. Every character is made up of an 8x8 pixel block. Thus, every character will require eight writes to external SRAM.

There are two special operations. A value of 0x80 will result in a clearscreen. During this operation the PIC will assert the CLEARING signal and then clear all the memory. A value of 0x0d is the newline character and will result in a newline on the video buffer. A value of 0x08 is the backspace character and will delete the previous character from the screen.

The CPLD runs at 25.175MHz and the PIC runs at 4MHz. The CPLD is the most power hungry device on Arbadell (which makes sense because it is the fastest) and consumes about 200mA.